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06EC46

Fourth Semester B.E. Degree Examination, January 2013
Linear IC's and Applications

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Sketch an illustration to show the effect of op-amp slew rate and explain. State a typical op-amp slew rate. **(05 Marks)**

b. An op-amp inverting amplifier has a 0.5 volts input signal and its output is to be 9 volts. If feed back resistor $R_f = 12\ K\Omega$, calculate a suitable resistance value for R_i. **(05 Marks)**

c. Explain why the resistances at the two input terminals of an op-amp should be approximately equal in value. **(04 Marks)**

d. A non-inverting amplifier is to amplify a 100 mV signal to a level of 3 volts, using a 741 op-amp, design a suitable circuit. Assume bias current as 500 nA (max). **(06 Marks)**

2 a. How to set the upper cut-off frequency in an inverting amplifier circuit? Explain. **(06 Marks)**

b. Discuss the significance of using single polarity supply in an op-amp circuits. **(06 Marks)**

c. A capacitor-coupled voltage follower is to be designed to have a lower cut-off frequency of 120 Hz. The load resistance is 8.2 KΩ and the op-amp used has a maximum input bias current of 600 nA. Design a suitable circuit. **(08 Marks)**

3 a. Sketch the circuit of a lead compensation network. Explain its operation. Show how it affects operational amplifier frequency response. **(08 Marks)**

b. Write a note on Z_{in} mod compensation. **(06 Marks)**

c. A 741 op-amp with a slew rate of 0.5 V/μ sec is used as a voltage follower:

i) Calculate the slew rate limited cut-off frequency if the sine wave output is 5 volts.

ii) If this circuit is to operate with a unity gain cut-off frequency of 800 kHz, calculate the maximum peak value of the sinusoidal output voltage.

iii) If the upper cut-off frequency is 8 kHz, calculate the maximum value of the peak output voltage. **(06 Marks)**

4 a. Draw the circuit of a precision voltage source using an op-amp and a zener diode. Explain the circuit operation and derive the equation relating to V_o and V_z. **(08 Marks)**

b. Show the realization of current to voltage converter using an op-amp. **(04 Marks)**

c. Design an instrumentation amplifier to have an overall voltage gain of 900. The input signal amplitude is 20 mV; 741 op-amps are to be used and the supply is ± 15V. **(08 Marks)**

PART – B

5 a. Show the realization of logarithmic amplifier using an op-amp. Obtain the expression for the output voltage. **(08 Marks)**

b. Sketch the circuit of a voltage follower type peak detector. Explain the circuit operation. **(06 Marks)**

c. Using 741 op-amp with a ± 9V supply design a phase shift oscillator to have an output frequency of 10 kHz. **(06 Marks)**

6 a. Draw the circuits to show how diodes may be used to select the trigger points of an inverting Schmitt trigger circuit. Explain. **(06 Marks)**

b. Sketch the circuit of a capacitor coupled zero-crossing detector. Show the waveforms at various points in the circuit and explain its operation. **(08 Marks)**

c. Design a second order low pass filter to have a cut-off frequency of 1.5 kHz, using 741 op-amp. **(06 Marks)**

7 a. Define and explain the terms as applied to voltage regulator:
   i) Line regulation
   ii) Load regulation
   iii) Ripple rejection. **(06 Marks)**

b. What is the principle of switch mode power supplies? Discuss the advantages and disadvantages. **(08 Marks)**

c. Explain the operation of switching regulator using op-amp. **(06 Marks)**

8 a. With a neat block schematic, explain the operation of each component in PLL. **(08 Marks)**

b. Write explanatory note on :
   i) 555 timer as monostable multivibrator
   ii) A/D converters. **(10 Marks)**

c. A PLL has free running frequency of 500 kHz and bandwidth of the low pass filter is 10 kHz. Will the loop acquire lock for an input signal of 600 kHz? Justify your answer. Assume that the phase detector produces sum and difference frequency components. **(02 Marks)**

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